CLAIMS

WHAT IS CLAIMED IS:

1. A transponder comprising:

a memory for storing data therein;

a clock generator for outputting a read signal for supplying current to the memory;

an address module for addressing an address in the memory, said clock generator outputting an address clock signal and said address module selecting an address to be read in response to a clock signal from said clock generator; and

a data module for receiving the data stored in said memory at an address indicated by said address module, said clock generator stopping supplying said read signal to turn off said current to said memory once said data has been output to said data module.

2. The transponder of claim 1, wherein said address clock signal is an increased address signal to said address module to change the address of said memory identified by said address module and said clock generator outputting the read signal to supply current to said memory when said increased address signal is supplied to said address module.

3. The transponder of claim 1, wherein said clock generator outputs a program signal for supplying current to the memory to program the memory, and said address clock signal is an address latch signal, the address module selecting a specific address of the memory in response to the address latch signal, said data module inputting data to the memory at the address indicated by the address module, said clock generator stopping supplying current to the memory once the data in the data module has been stored in the memory.

4. The transponder of claim 1, further comprising a program control and said memory having a status byte region and a data region, said program control reading data from said status byte region and in response thereto, outputting a program enable signal to said clock generator to enable said clock generator to output said address signal to said address module.

5. The transponder of claim 4, wherein said status byte region stores at least a first seal bit and a second seal bit, said program control reading said first seal bit and said second seal bit and outputting the program enable signal if at least one of said first seal bit and second seal bit is clear.

6. The transponder of claim 4, wherein said status byte includes an HLOCK bit, said HLOCK bit being capable of being set or clear, said program control reading said HLOCK bit and receiving an address from said address module, and outputting said program enable if said HLOCK bit is clear or said HLOCK bit is set and said address output by said address module corresponds to the address of the status byte within said memory.

7. A transponder comprising:

a memory for storing data therein, said memory having addresses;

a clock generator outputting a program signal for supplying current to the memory to program the memory;

an address module for addressing an address in the memory, said clock generator outputting an address latched signal, said address module selecting an address to be read in response to the address latch signal; and

a data module for inputting data to the memory at the address indicated by the address module, said clock generator stopping supplying current to the memory once the data in the data module has been stored in the memory.

8. The transponder of claim 7, further comprising a program control and said memory having a status byte region and a data region, said program control reading data from

said status byte region and in response thereto, outputting a program enable signal to said clock generator to enable said clock generator to output said address signal to said address module.

9. The transponder of claim 8, wherein said status byte region stores at least a first seal bit and a second seal bit, said program control reading said first seal bit and said second seal bit and outputting the program enable signal if at least one of said first seal bit and second seal bit is clear.

10. The transponder of claim 8, wherein said status byte includes an HLOCK bit, said HLOCK bit being capable of being set or clear, said program control reading said HLOCK bit and receiving an address from said address module, and outputting said program enable if said HLOCK bit is clear or said HLOCK bit is set and said address output by said address module corresponds to the address of the status byte within said memory.

11. The transponder of claim 1, wherein the clock generator outputs an address latch signal to said address module in response to a program signal from an interrogator, said address latch signal causing said address module to select an address to be programmed in accordance with said program signal, said program signal being pulse space modulated.

12. The transponder of claim 6, wherein said status byte further includes a mode bit, said program control reading said mode bit and providing an output to said address module preventing said address module from accessing addresses in said memory not corresponding to the mode indicated by said mode bit.

13. A transponder comprising:

a memory, said memory including a data region and a status byte region;

a clock generator for receiving a program signal and outputting a data latch signal in response thereto;

an address module for receiving said address latch signal and addressing a predetermined address in the memory to be programmed; and

a program control for reading said status byte and outputting a program enable signal in response thereto, said clock generator receiving said program enable signal and outputting said address latch in response to said program enable signal.

14. The transponder of claim 13, wherein said status byte region stores at least a first seal bit and a second seal bit, said program control reading said first seal bit and said second seal bit and outputting the program enable signal if at least one of said first seal bit and second seal bit is not set.

15. The transponder of claim 13, wherein said status byte includes an HLOCK bit, said HLOCK bit being capable of being set or clear, said program control reading said HLOCK bit and receiving an address from said address module, and outputting said program enable if said HLOCK bit is clear or said HLOCK bit is set and said address output by said address module corresponds to the address of the status byte within said memory.

16. A transponder for receiving an interrogator signal, the transponder comprising:

a comparator for receiving said interrogator signal and a reference voltage and outputting a first logic level if the voltage of the interrogator signal is greater than the reference voltage, and outputting a second logic level if the voltage of the interrogator signal is less than the reference voltage; and

a transmitter for receiving said first and second logic levels and outputting a first voltage indicator signal in response to said first logic level and outputting a second voltage indicator signal in response to said second voltage level, the first signal being the inverse of the second signal to indicate to an interrogator a received relative voltage level.

17. A memory for a transponder comprising a data region and a user lock region, said data region storing a plurality of characters;

said user lock region including a plurality of bits, the number of bits in said user lock region at least equaling the number of characters in said data region, each bit of said user lock region corresponding to a respective character, each of said bits in said user

lock region indicating a locked or unlocked status of said respective character in said data region.

18. The memory of claim 17, wherein said data region is formed as a plurality of bits, a subsets of said bits representing a respective character of said plurality of said characters, and each bit of said user lock region corresponding to a respective subset of bits.

19. The transponder of claim 17, wherein said memory further comprises a status byte region, said status byte region storing data indicating that said data region is locked.

20. The transponder of claim 19, wherein said status byte region includes a first seal and a second seal, wherein at least said data region is not permanently locked if at least one of said first seal and said second seal are clear.

21. The transponder of claim 19, wherein said status byte includes an HLOCK region for locking at least the data stored in the said data region.

22. The transponder of claim 19, wherein said status byte includes a mode bit for indicating the mode under which the memory shall be operated upon.

23. A memory for a transponder comprising a data region and a status byte region, the status byte region including at least a permanent lock indicator, said permanent lock indicator exhibiting one of a set state or clear state, said permanent lock indicator exhibiting a clear state indicating that said memory can be programmed.

24. The memory of claim 23, wherein said status byte further comprises an HLOCK bit, said HLOCK bit being capable of being set or clear, to indicate whether at least said data region can be programmed.

25. The memory of claim 23, wherein said status byte further comprises a mode bit, said mode bit indicating which addresses of said memory can be operated upon.

26. The memory of claim 23, further comprising a user lock region, said data region storing the plurality of characters, said user lock region including a plurality of bits, the number of bits in said user lock region at least equaling the number of characters in said data

region, each bit of said user lock region corresponding to respective character, each of said bits in said user lock region indicate a locked or unlocked status of said respective character in said data region.

27. The memory of claim 26, wherein said data region stores a plurality of bits, said plurality of characters being represented by respective pluralities of subsets of said bits, the number of bits in said user lock region at least equaling the number of said subsets of bits in said data region.

28. The memory for a transponder as claimed in claim 23, wherein said permanent lock indicator includes a first seal bit and a second seal bit, said first seal bit and second seal bit exhibiting one of a clear state and set state, at least one of said first bit or second bit indicating a clear state indicating that the data in the data region can be programmed.

29. A method for selectively allowing reprogramming of a transponder memory comprising the steps of:

providing a data region within said memory, the data region including a plurality of characters;

providing a user lock region within said memory, said user lock region having at least as many bits as said plurality of characters in said data region, each bit of said user lock region corresponding to a respective character in said data region; and

setting the bits in the user lock corresponding to the characters in said data region which cannot be reprogrammed.

30. The method of claim 29, wherein said data region includes a plurality of bits, a subset of said bits corresponding to a respective character, and each bit of said user lock region corresponding to a respective subset of bits.

31. The method of claim 29, for selectively allowing reprogramming of a transponder memory further comprising the steps of:

reading data stored in said data region and user lock region from said memory;

determining whether or not a character in the data region to be programmed has a corresponding set bit in said user lock region;

programming the character to be programmed if the corresponding bit in the user lock region is clear; and

not programming the character to be programmed in the data region if the corresponding bit in the user lock region is set.

32. The method of claim 31, further comprising the step of clearing said set bit in the user lock region before programming the corresponding character in said data region.

33. The method of claim 32, further comprising the step of resetting the bit of the user lock region corresponding to the programmed character in the data region.

34. The method of claim 31, further comprising the steps of providing a status byte region in said memory, said status byte region including a first seal bit and a second seal bit; and

reading said bits in said status byte region and preventing programming of the character in said data region if said first seal and second seal bits indicate a lock condition.

35. The method of claim 31, wherein said memory includes a status byte region, said status byte region including an HLOCK bit and further comprising the steps of:

reading said HLOCK bit from the memory; and

preventing programming said character in the data region if the HLOCK bit is set.

36. The method of claim 31, further comprising the step of reading the bits stored in the data region and user lock region;

comparing the character in the data region to be programmed with a character of data to be programmed into the memory;

determining whether the character to be programmed and the character stored in the memory are different;

not programming the data if the characters are the same; and

if the characters are not the same, determining whether or not the corresponding bit in the user lock region is set.

37. A method for determining temperature from a transponder utilizing a thermistor and a running counter comprising the steps of:

providing a running count which varies as a function of temperature;

latching the count at predetermined time intervals;

determining the difference between the values of successive latched counts;

aggregating the differences;

determining the total elapsed time between a first latched count and a last latched count;

dividing the aggregate by the total time to obtain a frequency; and

converting the frequency to a temperature based upon the temperature frequency characteristics of the thermistor.

38. The method of claim 37, comprising the step of determining the difference between the smallest difference obtained and the largest difference obtained and determining whether or not the second difference falls within a range;

beginning the process over if the difference does not fall within the range.

39. The method of claim 38, further comprising repeating the steps to obtain a second temperature value;

comparing a first temperature value to the second temperature value; and

outputting the temperature as a temperature value if the first temperature value is equal to the second temperature value.

40. A method for checking the integrity of a signal received from a transponder utilizing an accumulator comprising the steps of:

receiving a first data bit from a transponder;

receiving a next data bit from a transponder;

calculating the actual time elapsed between the last two successive data bits;

subtract an average time expected between data bits from the actual time between data bits to produce an error amount;

add the error amount to the accumulator;

determine whether or not an accumulated value is greater than a predetermined error detection constant; and

stop receiving transponder data bits if the accumulator value is greater than the error detection constant.

41. An interrogator, said interrogator outputting a command signal corresponding to a process to be performed by a transponder, said command signal being a pulse width modulated signal.

42. The interrogator of claim 41, wherein said transponder includes a memory and said command signal causes data to be programmed into said memory.

43. The interrogator of claim 41, wherein said command signal causes said transponder to output a temperature.

44. The transponder of claim 1, wherein said transponder is formed as an integrated circuit and further comprising a clamp, the clamp including at least one MOSFET.

45. The transponder of claim 44, wherein said clamp is formed by a CMOS process.

46. A transponder for receiving power from an outside power source comprising an Integrated Circuit, said integrated circuit including a clamp, the clamp including at least one MOSFET.

47. The transponder of claim 46, wherein said clamp is formed in a CMOS process.

09502696 - 021709